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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,548	JAYARAMAN ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-19 and 21-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17-19 and 21-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 10, 11, 14, 17-19 and 21-25 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,259,155 (Interrtante).

Interrante discloses, referring to figures 4A-5B, an electronic assembly comprising; a circuit board (40); a package substrate (30), having first and second sides, attached to the circuit board; a plurality of electrical contact formations (32) on the first side of the package substrate electrically interconnecting the circuit board and the package substrate; a stress relief layer (50) on the first side of the package substrate and contracting the plurality of electrical contact formations, a space being defined between the stress relief layer and the circuit board (see col. 3, lines 5-40); and a microelectronic die (20), having an integrated circuit formed therein, mounted on the second side of the package substrate [**claim 1**] , wherein each of the plurality of electrical contact formations has a height and the stress relief layer has a thickness, the thickness of the stress relief layer (see col. 3, lines 35-40) being less than the height of the plurality of contact formations (see col. 3, lines 10-15) [**claim 2**], wherein the stress relief layer is adjacent to a portion of the plurality of electrical contact formations that corresponds to only a portion of the height of the contact formations (see figure 1)

[**claim 3**], wherein the heights of the plurality of electrical contact formations are between 0.2 and 1.5 mm (see col. 3, lines 10-15) [**claim 4**], wherein the stress relief layer is polymeric (see col. 3, lines 30-35) [**claim 5**], wherein the stress relief layer is an adhesive paste (see col. 3, lines 55-65) [**claim 6**].

Similarly, Interrante discloses, an electronic assembly, comprising: a package substrate (30) having first and second sides; a microelectronic die (20) mounted to the first side of the package substrate; a plurality of electrical contact formations (32) attached to the second side of the package substrate, each having a height and configured to electrically interconnect; and a stress relief layer (50) on the second side of the package substrate in contact with the plurality of electrical contact formations, the layer having a thickness (see col. 3, lines 10-15) less than the height of the contact formations (see col. 3, lines 35-40) and being adjacent to only a portion of the height of the plurality of contact formations (see fig. 5B) [**claim 10**], wherein the microelectronic die is a microprocessor (see col. 1, lines 10-15) [**claim 11**].

Additionally, Interrante discloses, referring primarily to figures 4A-5B, an electronic assembly comprising; a circuit board (40); a package substrate (30), having first and second sides, attached to the circuit board; a plurality of electrical contact formations (32) on the first side of the package substrate electronically interconnecting the circuit board and the package substrate; a stress relief layer (50) between the package substrate and the circuit board and in contact with the plurality of electrical connections; and a microprocessor (20, see col. 1, lines 10-15), mounted on the second side of the package substrate [**claim 14**].

Furthermore, Interrante discloses, referring primarily to figures 4A-5B, a method of constructing an electronic assembly, comprising: depositing a stress relief layer (50) on a side of a package substrate (30), the side having a plurality of electrical contact formations (32) thereon; such that the stress relief layer comes in contact with the plurality of electrical contact formations, and attaching the contact formations to a circuit board (40), a space being defined between the stress relief layer and the circuit board [**claim 17**], wherein a microelectronic die (20) is mounted on an opposing side of the package substrate [**claim 18**], wherein the contacts have a height (see col. 3, lines 10-15) and the stress relief layer has a thickness (see col. 3, lines 35-40), the thickness of the stress relief layer being less than the height of the plurality of electrical contact formations [**claim 19**], wherein the stress relief layer is polymeric [**claim 21**], wherein the stress relief layer is only deposited onto selected portions of the side of the package substrate (see figure 4B) [**claim 22**], wherein the stress relief layer flows onto the package substrate (see col. 3, lines 35-45) [**claim 23**], wherein the stress relief layer is first deposited onto a central portion of the side of the package substrate (see col. 3, lines 35-45) [**claim 24**], wherein the stress relief layer is extruded onto the side of the side of the package substrate (see col. 3, lines 35-45) [**claim 25**].

Claims 1-8, 10, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,372,547 (Nakamura1).

Nakamura1 discloses, referring to figure 2, an electronic assembly comprising; a circuit board (8); a package substrate (1), having first and second sides, attached to the

circuit board; a plurality of electrical contact formations (4) on the first side of the package substrate electrically interconnecting the circuit board and the package substrate; a stress relief layer (5) on the first side of the package substrate and contracting the plurality of electrical contact formations, a space being defined between the stress relief layer and the circuit board; and a microelectronic die (3), having an integrated circuit formed therein, mounted on the second side of the package substrate [**claim 1**] , wherein each of the plurality of electrical contact formations has a height and the stress relief layer has a thickness, the thickness of the stress relief layer being less than the height of the plurality of contact formations (see col. 2, lines 45-50) [**claim 2**], wherein the stress relief layer is adjacent to a portion of the plurality of electrical contact formations that corresponds to only a portion of the height of the contact formations (see col. 2, lines 45-50) [**claim 3**], wherein the heights of the plurality of electrical contact formations are between 0.2 and 1.5 mm (see col. 6, lines 25-35) [**claim 4**], wherein the stress relief layer is polymeric (see col. 2, lines 50-55) [**claim 5**], wherein the stress relief layer is an adhesive paste (see col. 2, lines 50-55) [**claim 6**], wherein the thickness of the stress relief layer is between 0.15 and 0.225 mm (see col. 2, lines 50-55) [**claim 7**], wherein the space is an air space [**claim 8**].

Also, Nakamura1 discloses, referring primarily to figure 2, an electronic assembly, comprising: a package substrate (20) having first and second sides; a microelectronic die (3) mounted to the first side of the package substrate; a plurality of electrical contact formations (2) attached to the second side of the package substrate, each having a height and configured to electrically interconnect; and a stress relief layer

(5) on the second side of the package substrate in contact with the plurality of electrical contact formations, the layer having a thickness less than the height of the contact formations (see col. 2, lines 45-50) and being adjacent to only a portion of the height of the plurality of contact formations (see col. 2, lines 45-50) [**claim 10**].

Additionally, Nakamura1 discloses, a method of constructing an electronic assembly comprising depositing a stress relief layer (5) on a side of a package substrate, the side having a plurality of contact formation (2) thereon, wherein the stress relief layer is a cast film, having a plurality of holes therein, and said depositing is placing the cast film on the side of the package substrate so that the contact formations extend through the holes (see col. 6, lines 30-50), and attaching the contact formations to a circuit board (8), a space being defined between the stress relief layer and the circuit board [**claim 26**].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura1 in view of Interrante.

Nakamura1 discloses the claimed invention as described above with respect to claim 8, except Nakamura1 does not specifically state that the microelectronic die is a microprocessor [**claim 9**]. However, it is well known in the art that microprocessors are a subset of microelectronic dice as evidenced by Interrante (see col. 1, lines 10-15). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a microprocessor as the microelectronic die in the invention of Nakamura as is well known in the art and evidenced by Interrante. The motivation for doing so would have been to make the device suitable to a computer environment.

Similarly, Nakamura1 discloses the claimed invention as described above with respect to claim 10, except Nakamura1 does not specifically state that the

microelectronic die is a microprocessor [**claim 11**]. However, it is well known in the art that microprocessors are a subset of microelectronic dice as evidenced by Interrante (see col. 1, lines 10-15). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a microprocessor as the microelectronic die in the invention of Nakamura as is well known in the art and evidenced by Interrante. The motivation for doing so would have been to make the device suitable to a computer environment. Moreover, the modified invention of Nakamura1 teaches wherein the plurality of electrical contact formations are BGA solder balls (see col. 1, lines 20-25) [**claim 12**], wherein the stress relief layer is polymeric (see col. 2, lines 50-55) [**claim 13**].

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura1 in view of US 6,219,241 (Jones).

Nakamura1 discloses the claimed invention as described above with respect to claim 10, except Nakamura1 does not specifically state that the circuit board is a motherboard [**claim 15**]. However it is well known in the art that PCBs may comprise motherboards as evidenced by Jones (see col. 1, lines 10-25). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a motherboard as the PCB in the modified invention of Lo as is well known in the art and evidenced by Jones. The motivation for doing so would have been to make the device suitable to a computer environment

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,706,558 (Nakamura2) in view of Nakamura1.

Nakamuras discloses, referring primarily to figure 6A, a method comprising: placing a plurality of semiconductor packages on a support (11) the semiconductor packages each having a package substrate (14) with a first side having a microelectronic die (17) mounted thereon and a second side with a plurality of electrical contact formations connected thereto (23), the plurality of electrical contact formations having a height. Nakamura does not specifically disclose suspending a stencil over the semiconductor packages, the stencil having a plurality of holes; and flowing a paste through the holes of the stencil to form a stress relief layer on the second side of the package substrate of each semiconductor package, the stress relief layer having a thickness, the thickness being less than the height of the contact formations. However, Nakamura1 teaches depositing a stress relief layer on package substrates to a height less than contact formations (see col. 2, lines 45-50). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to deposit the stress relief layer taught by Nakamura1 onto the invention of Nakamura2. The motivation for doing so would have been to absorb thermal stress to prevent the electrodes from cracking when bonding. Additionally, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use screen printing (stencils) as the method of relief layer deposition, since Nakamura teaches this is an effective process for selective deposition (see col. 5, lines 50-60) [**claim 27**]. The

motivation for doing so would have been to use a simple process that can form all the relief layers simultaneously, thus reducing the required processing time.

The combined disclosures of Nakamura2 and Nakamura1 additionally teach, further comprising placing the semiconductor packages onto circuit boards, the contact formations interconnecting the package substrates and the circuit board, a space being defined between the circuit board and the second side of the package substrate (see Nakamura1 figure 2) [**claim 28**], wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations (see Nakamura1 col. 2, lines 45-50) [**claim 29**], wherein the second sides of the package substrates face the stencil (see Nakamura2 col. 5, lines 50-60) [**claim 30**].

Allowable Subject Matter

The indicated allowability of claim 26 is withdrawn in view of the amendments to the claim which have removed/changed limitations and thus the meets and bounds of the claim.

Response to Arguments

Applicant's arguments with respect to claims 1-15, 17-19,21-30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN